ADCTRIG PAGE 1

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3 ; Author : ADI - Apps

4 ;

5 ; Date : January 2001

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7 ; File : ADCtrig.asm

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9 ; Hardware : ADuC816

10 ;

11 ; Description : Flash led an initial rate of 100ms

12 ; Pressing INTO triggers single conversion

13 ; The ADC result is written to external memory

14 ; The delay rate is increased

15 ; The program waits for the next INTO to repeat the

16 ; above sequence

17 ;

18 ;======================================================================

19 ;

20 $MOD816 ; Use ADuC816 predefined Symbols

21

0000 22 FLAG EQU 00H ; Define Bit

23

---- 24 CSEG ; Defines the following as a segment of code

25

0000 26 ORG 0000H ; Load Code at '0'

27

0000 020057 28 JMP MAIN ; Jump to MAIN

29

30 ;======================================================================

31 ; (INT0 ISR)

0003 32 ORG 0003h

0003 F5F0 33 MOV B,A ; Copy A (sets delay)

0005 04 34 INC A ; Increment delay

35

0006 75D122 36 MOV ADCMODE,#22H ; Initiate a PRIM ADC single conv

37

0009 30DFFD 38 JNB RDY0,$ ; Wait for conversion results

39

40 ; Write ADC Result H/M to ext. memory

000C E5DA 41 MOV A,ADC0M ; read ADC Middle byte

000E F0 42 MOVX @DPTR,A ; write Middle byte to ext memory

000F A3 43 INC DPTR

0010 E5DB 44 MOV A,ADC0H ; read ADC High byte

0012 F0 45 MOVX @DPTR,A ; write low High byte to ext memory

0013 A3 46 INC DPTR

47

0014 E5F0 48 MOV A,B ; Restore A (sets delay)

0016 04 49 INC A ; Increment delay

50

0017 32 51 RETI ; Return from Interrupt

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55

004B 56 ORG 004Bh ; Subroutines

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58 ;------------------------------------------------------------------

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59

004B 60 DELAY: ; Delays by 100ms \* A

61

004B F8 62 MOV R0,A ; Acc holds delay variable

004C 7919 63 DLY0: MOV R1,#019h ; Set up delay loop0

004E 7AFE 64 DLY1: MOV R2,#0FEh ; Set up delay loop1

0050 DAFE 65 DJNZ R2,$ ; Dec R2 & Jump here until R2 is 0

0052 D9FA 66 DJNZ R1,DLY1 ; Dec R1 & Jump DLY1 until R1 is 0

0054 D8F6 67 DJNZ R0,DLY0 ; Dec R0 & Jump DLY0 until R0 is 0

0056 22 68 RET ; Return from subroutine

69

70 ;======================================================================

71

0057 72 MAIN: ; (main program)

73

74 ; Configure ADC

0057 75D120 75 MOV ADCMODE,#20H ; ENABLE MAIN ADC; Mode- Power down

005A 75D247 76 MOV ADC0CON,#47H ; 24 BITS

77 ; USE EXTERNAL REFERENCE

78 ; AIN1-AIN2

79 ; BIPOLAR MODE

80 ; RANGE = +/-2.56V

81

005D D288 82 SETB IT0 ; INT0 edge triggered

005F D2AF 83 SETB EA ; enable inturrupts

0061 D2A8 84 SETB EX0 ; enable INT0

0063 C200 85 CLR FLAG ; Clear Bit defined as FLAG

86

0065 7401 87 MOV A,#01H ; Initialize A -> 1

0067 B2B4 88 BLINK: CPL P3.4 ; blink LED using compliment instruction

0069 114B 89 CALL DELAY ; Jump to subroutine DELAY

006B 3000F9 90 JNB FLAG,BLINK ; If FLAG is still cleared the jump to Blink

91

92 END

93

94

95

VERSION 1.2h ASSEMBLY COMPLETE, 0 ERRORS FOUND

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ADC0CON. . . . . . . . . . . . . D ADDR 00D2H PREDEFINED

ADC0H. . . . . . . . . . . . . . D ADDR 00DBH PREDEFINED

ADC0M. . . . . . . . . . . . . . D ADDR 00DAH PREDEFINED

ADCMODE. . . . . . . . . . . . . D ADDR 00D1H PREDEFINED

B. . . . . . . . . . . . . . . . D ADDR 00F0H PREDEFINED

BLINK. . . . . . . . . . . . . . C ADDR 0067H

DELAY. . . . . . . . . . . . . . C ADDR 004BH

DLY0 . . . . . . . . . . . . . . C ADDR 004CH

DLY1 . . . . . . . . . . . . . . C ADDR 004EH

EA . . . . . . . . . . . . . . . B ADDR 00AFH PREDEFINED

EX0. . . . . . . . . . . . . . . B ADDR 00A8H PREDEFINED

FLAG . . . . . . . . . . . . . . NUMB 0000H

IT0. . . . . . . . . . . . . . . B ADDR 0088H PREDEFINED

MAIN . . . . . . . . . . . . . . C ADDR 0057H

P3 . . . . . . . . . . . . . . . D ADDR 00B0H PREDEFINED

RDY0 . . . . . . . . . . . . . . B ADDR 00DFH PREDEFINED